Digital version

ENGS152 Circuits Lab
MOSFET logic gates

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Step 1: AND gate

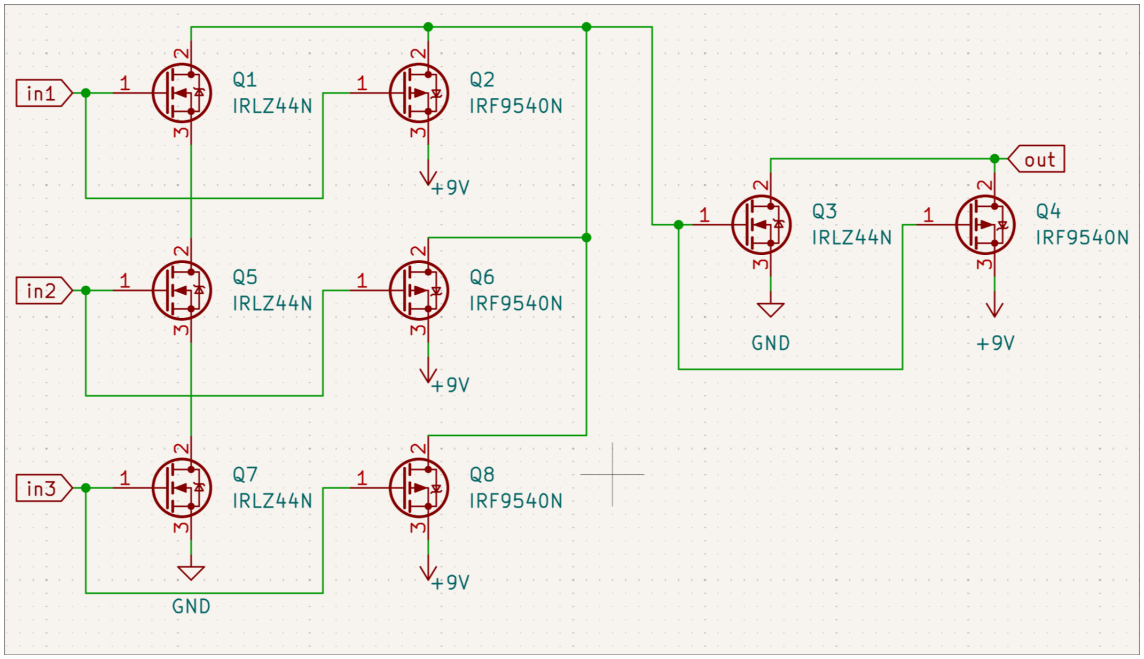

Figure 1: AND gate schematic

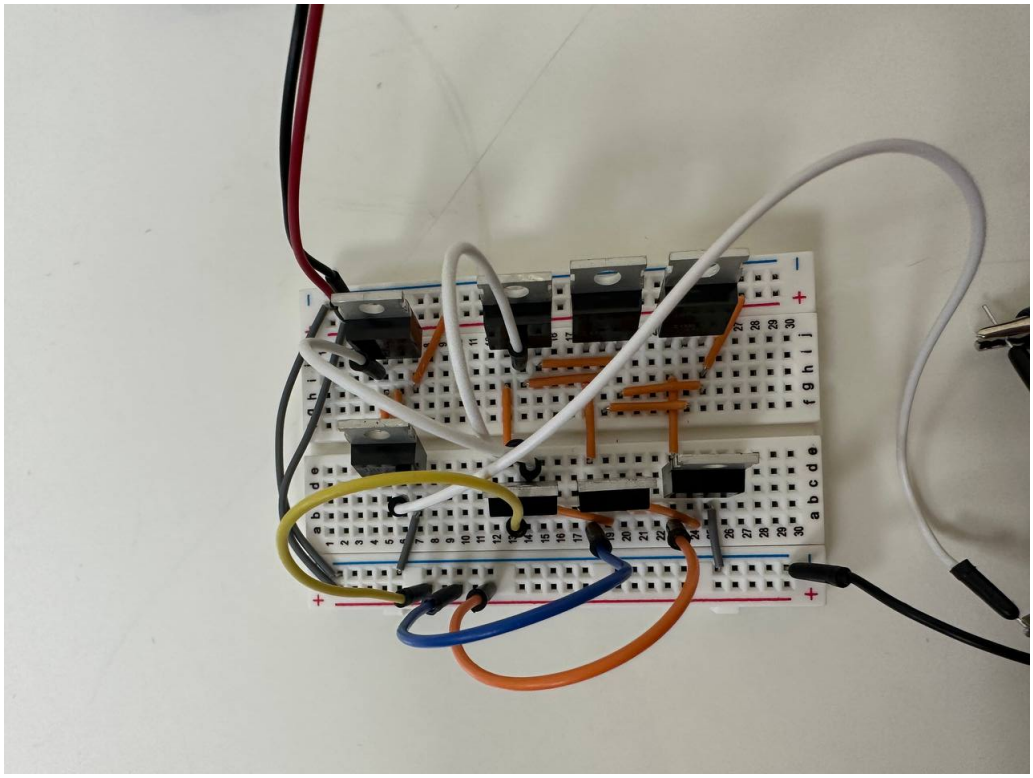

Figure 2: AND gate circuit

m	s	l	o
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Table 1: Truth table for AND gate

We chose a NAND gate connected to a NOT gate, to make an AND gate.

Step 2: OR gate

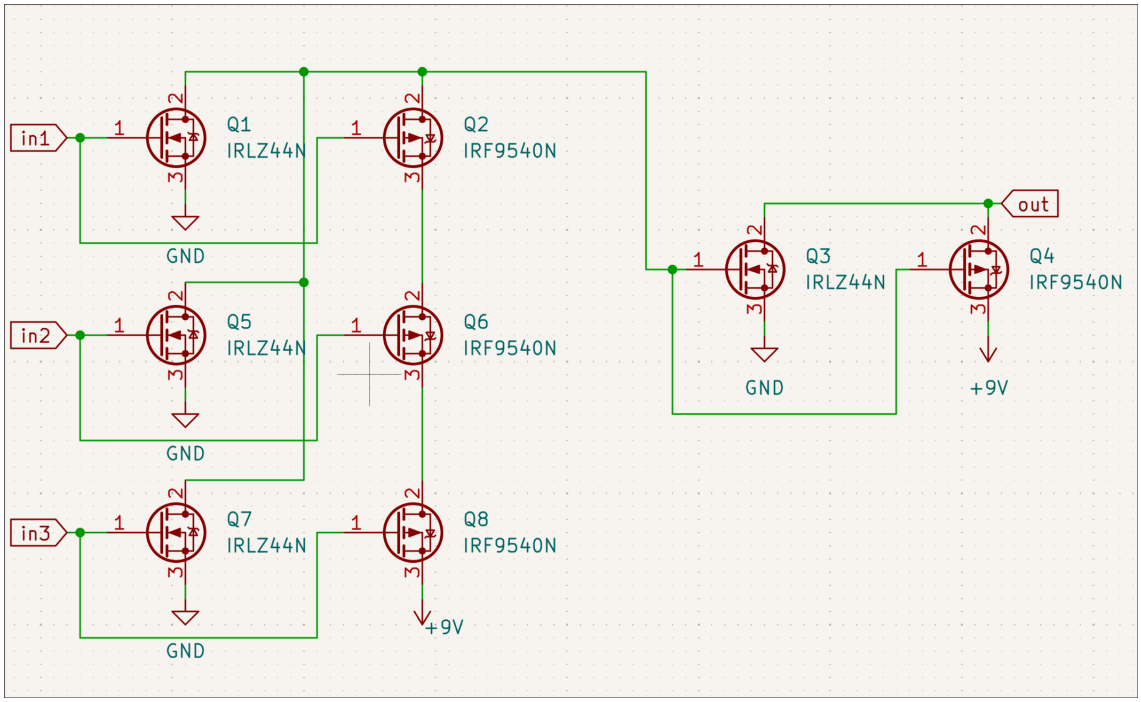

Figure 3: OR gate schematic

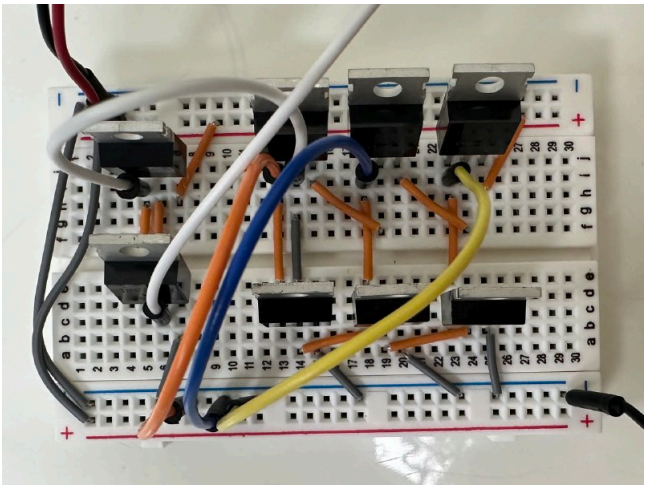

Figure 4: OR gate circuit

m	s	l	o
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

Table 2: Truth table for OR gate

We chose a NOR gate connected to a NOT gate, to make an OR gate.